Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A power supply clamp circuit for preventing damage to integrated circuits when electrostatic discharge occurs at a first voltage source of the integrated circuits, the power supply clamp circuit comprising:

a first voltage generator electrically connected to a first node for generating a voltage;

a first PMOS transistor having a source electrically connected to the first voltage source, a gate electrically connected to the first node, and a drain electrically connected to a second node;

a first NMOS transistor having a drain electrically connected to the second node, a gate electrically connected to the first node, and a source connected to ground;

a second NMOS transistor having a drain electrically connected to the first voltage source, a gate electrically connected to the second node, and a source connected to ground; and

a second PMOS transistor having a source electrically connected to the second node, a gate and a drain both electrically connected to the first node.

[c2] 2. The power supply clamp circuit of claim 1 wherein a drain of the second NMOS transistor of the power supply clamp circuit has P+ implantation dosage in an ion implantation process.

[c3] 3. The power supply clamp circuit of claim 1 wherein the first voltage generator of the power supply clamp circuit comprises:
a resistor having one end of the resistor electrically connected to the first voltage source and another end of the resistor electrically connected to the first node; and
a capacitor having one end of the capacitor electrically connected to the first node and another end of the capacitor connected to ground.

[c4] 4. The power supply clamp circuit of claim 3 wherein the resistor of the first voltage generator comprises metal wiring.

[c5] 5. The power supply clamp circuit of claim 3 wherein the capacitor of the first voltage generator comprises an NMOS transistor having a drain and a gate electrically connected to a substrate.

[c6] 6. The power supply clamp circuit of claim 1 wherein the integrated circuits of the power supply clamp circuit further comprise a second voltage source that is indepen-

dent from the first voltage source but with the same voltage as the first voltage source, the second voltage source comprising:
a resistor with one end of the resistor electrically connected to the second voltage source andanother end of the resistor electrically connected to a third node;
a third PMOS transistor having a source electrically connected to the third node, a gateelectrically connected to afourth node, and a drain electrically connected to the first node; and
a third NMOS transistor having a drain and a gate commonly electrically connected to the fourth node, and a source connected to ground.

[c7] 7.The power supply clamp circuit of claim 6 wherein a drain of the second NMOS transistor of the power supply clamp circuit has P+ implantation dosage in an ion implantation process.

[c8] 8. The power supply clamp circuit of claim 6 wherein the resistor of the second voltage source comprises metal wiring.

[c9] 9. A power supply clamp circuit for preventing damage to integrated circuits when electrostatic discharge occurs at a first voltage source of the integrated circuits, the power supply clamp circuit comprising:

a first PMOS transistor having a source electrically connected to the first voltage source, a gate electrically connected to a first node, and a drain electrically connected to a second node;

a first NMOS transistor having a drain electrically connected to the second node, a gate electrically connected to the first node, and a source connected to ground;

a second NMOS transistor having a drain electrically connected to the first voltage source, a gate electrically connected to the second node, and a source connected to ground;

a second voltage source being independent from a first voltage source and having the same voltage as the first voltage source;

a resistor with one end of the resistor electrically connected to thesecond voltage source andanother end of the resistor electrically connected to athird node;

a third PMOS transistor having a source electrically connected to thethird node, a gateelectrically connected to afourth node, and a drain electrically connected to the first node; and

a third NMOS transistor having a drain and a gate commonly electrically connected to the fourth node, and a source connected to ground.

[c10] 10. The power supply clamp circuit of claim 8 wherein

the drain of the second NMOS transistor of the power supply clamp circuit has P+ implantation dosage in an ion implantation process.

[c11] 11. The power supply clamp circuit of claim 8 wherein the resistor of the power supply clamp circuit comprises metal wiring.